

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A read channel, comprising:
 2. an equalizer configured to equalize a digital signal to provide equalized
 3. reproduced signals; and
 4. a Viterbi detector capable of receiving the equalized reproduced signals and
 5. converting the reproduced signals into a digital output signal indicative of data stored on
 6. a recording medium;
7. wherein the equalizer is implemented using a coefficient learning circuit that
8. adaptively updates coefficients for the equalizer based upon a cosine function, the
9. coefficient learning circuit adjusting coefficients using a tap coefficient update equation
10. having a first parameter, k, for modifying a magnitude response, wherein the first
11. parameter, k, is adjusted according to $k = k - g * (f(a_{k+1}) + f(a_{k-1})) * e_k$, where k is the cosine
12. equalizer parameter for modifying the magnitude response, g is an update attenuation
13. gain, f() is a predetermined cosine function, a_{k+1} represents a bit to be detected at time
14. $k+1$, a_{k-1} represents a bit to be detected at time $k-1$, and e_k is an error signal based on a
15. difference between a noisy equalized signal and a desired noiseless signal.

1. 2-3. (Canceled)

1 4. (Currently Amended) The read channel of claim [[2]] 1, wherein the
2 coefficient learning circuit adjusts coefficients using a tap coefficient update equation
3 having a second parameter, j, for modifying a phase response.

1 5. (Previously Presented) The read channel of claim 4, wherein the
2 second parameter, j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where j is the
3 cosine equalizer parameter for modifying the phase response, g is an update attenuation
4 gain, f() is a predetermined cosine function, a_{k+2} represents a bit to be detected at time
5 k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error signal based on a
6 difference between a noisy equalized signal and a desired noiseless signal.

1 6. (Canceled)

1 7. (Currently Amended) The read channel of claim 1 A read channel,
2 comprising:
3 an equalizer configured to equalize a digital signal to provide equalized
4 reproduced signals; and
5 a Viterbi detector capable of receiving the equalized reproduced signals and
6 converting the reproduced signals into a digital output signal indicative of data stored on
7 a recording medium;
8 wherein the equalizer is implemented using a coefficient learning circuit that
9 adaptively updates coefficients for the equalizer based upon a cosine function, wherein
10 the coefficient learning circuit adjusts coefficients, w_i , according to $w_i = w_i - g * f(a_{k-i}) * e_k$,
11 where g is a provided update attenuation gain and $f(\cdot)$ is a predetermined
12 cosine function and a_{k+i} represents a bit to be detected at time $k+i$. a_{k-i}

1 8. (Original) The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be
2 $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i} , are convolved with a PR4
3 response based upon the cosine function.

1 9. (Original) The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be
2 $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are convolved
3 with the EPR4 response based upon the cosine function.

1 10. (Original) The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be
2 $a_{k-i}t_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with t_k based upon
3 the cosine function.

1 11. (Original) The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be
2 $a_{k-i}h_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with h_k based upon
3 the cosine function.

1 12. (Currently Amended) A waveform equalizer that equalizes a waveform of
2 a reproduction signal obtained by reproducing marks and non-marks recorded on a
3 recording medium, comprising:
4 a delay element that delays a propagation of the reproduced signal;
5 a plurality of multipliers that multiply predetermined coefficients by the
6 reproduction signal and the delayed signal from the delay element;
7 a coefficient learning circuit that adaptively updates the predetermined
8 coefficients for each of the plurality of multipliers; and
9 an adder that adds outputs from the plurality of multipliers;
10 wherein the coefficient learning circuit adaptively updates coefficients for the
11 equalizer based upon a cosine function, the coefficient learning circuit adjusting
12 coefficients using a tap coefficient update equation having a first parameter, k, for
13 modifying a magnitude response, wherein the first parameter, k, is adjusted according to
14 $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k is the cosine equalizer parameter for modifying the
15 magnitude response, g is an update attenuation gain, f() is a predetermined cosine
16 function, a_{k+1} represents a bit to be detected at time k+1, a_{k-1} represents a bit to be
17 detected at time k-1, and e_k is an error signal based on a difference between a noisy
18 equalized signal and a desired noiseless signal.

1 13-14. (Canceled)

1 15. (Currently Amended) The waveform equalizer of claim [[13]] 12,
2 wherein the coefficient learning circuit adjusts coefficients using a tap coefficient update
3 equation having a second parameter, j, for modifying a phase response.

1 16. (Previously Presented) The waveform equalizer of claim 15,
2 wherein the second parameter, j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where
3 j is the cosine equalizer parameter for modifying the phase response, g is an update
4 attenuation gain, f() is a predetermined cosine function, a_{k+2} represents a bit to be
5 detected at time k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error
6 signal based on a difference between a noisy equalized signal and a desired noiseless
7 signal.

1 17. (Canceled)

1 18. (Currently Amended) The waveform equalizer of claim 12 A waveform
2 equalizer that equalizes a waveform of a reproduction signal obtained by reproducing
3 marks and non-marks recorded on a recording medium, comprising:
4 a delay element that delays a propagation of the reproduced signal;
5 a plurality of multipliers that multiply predetermined coefficients by the
6 reproduction signal and the delayed signal from the delay element;
7 a coefficient learning circuit that adaptively updates the predetermined
8 coefficients for each of the plurality of multipliers; and
9 an adder that adds outputs from the plurality of multipliers;
10 wherein the coefficient learning circuit adaptively updates coefficients for the
11 equalizer based upon a cosine function, wherein the coefficient learning circuit adjusts
12 coefficients, w_i , according to $w_i = w_i - g * f(a_{k-i}) * e_k$, where g is a provided update attenuation
13 gain and and $[f(a_{k-i})]$ $f(\cdot)$ is a predetermined cosine function and $[a_{k+i}]$ a_{k-i} represents
14 a bit to be detected at time $[k+I]$ $k-i$.

1 19. (Original) The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i} , are convolved
3 with a PR4 response based upon the cosine function.

1 20. (Original) The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are
3 convolved with the EPR4 response based upon the cosine function.

1 21. (Original) The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i}t_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with t_k
3 based upon the cosine function.

1 22. (Original) The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i}h_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with h_k
3 based upon the cosine function.

1 23. (Currently Amended) A signal processing system, comprising:
2 memory for storing data therein; and
3 a processor, coupled to the memory, for equalizing a digital signal to provide
4 equalized reproduced signals, the processor adaptively updates coefficients for the
5 equalizer based upon a cosine function, the processor adjusting coefficients using a tap
6 coefficient update equation having a first parameter, k, for modifying a magnitude
7 response, wherein the first parameter, k, is adjusted according to $k = k - g * (f(a_{k+1}) + f(a_{k-1})) * e_k$,
8 where k is the cosine equalizer parameter for modifying the magnitude response, g
9 is an update attenuation gain, f() is a predetermined cosine function, a_{k+1} represents a bit
10 to be detected at time k+1, a_{k-1} represents a bit to be detected at time k-1, and e_k is an
11 error signal based on a difference between a noisy equalized signal and a desired
12 noiseless signal.

1 24-25. (Canceled)

1 26. (Currently Amended) The signal processing system of claim [[24]] 23,
2 wherein the processor adjusts coefficients using a tap coefficient update equation having
3 a second parameter, j, for modifying a phase response.

1 27. (Previously Presented) The signal processing system of claim 26,
2 wherein the second parameter, j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where
3 j is the cosine equalizer parameter for modifying the phase response, g is an update
4 attenuation gain, f() is a predetermined cosine function, a_{k+2} represents a bit to be
5 detected at time k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error
6 signal based on a difference between a noisy equalized signal and a desired noiseless
7 signal.

1 28. (Canceled)

1 29. (Currently Amended) The signal processing system of claim 23 A signal
2 processing system, comprising:
3 memory for storing data therein; and
4 a processor, coupled to the memory, for equalizing a digital signal to provide
5 equalized reproduced signals, the processor adaptively updates coefficients for the
6 equalizer based upon a cosine function, wherein the coefficient learning circuit adjusts
7 coefficients, w_i , according to $w_i=w_i-g*f(a_{k-i})*e_k$, where g is a provided update attenuation
8 gain and and [[f(a_{k-i})]] f() is a predetermined cosine function and [[a_{k+i}]] a_{k-i} represents
9 a bit to be detected at time [[k+I]] k-i.

1 30. (Original) The signal processing system of claim 29, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i}-a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i} , are convolved
3 with a PR4 response based upon the cosine function.

1 31. (Original) The signal processing system of claim 29, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are
3 convolved with the EPR4 response based upon the cosine function.

1 32. (Original) The signal processing system of claim 29, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i}t_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with t_k
3 based upon the cosine function.

1 33. (Original) The signal processing system of claim 29, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i}h_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with h_k
3 based upon the cosine function.

1 34. (Currently Amended) A magnetic storage device, comprising:

2 a magnetic storage medium for recording data thereon;

3 a motor for moving the magnetic storage medium;

4 a head for reading and writing data on the magnetic storage medium;

5 an actuator for positioning the head relative to the magnetic storage medium; and

6 a data channel for processing encoded signals on the magnetic storage medium,

7 the data channel comprising an equalizer configured to equalize a digital signal to

8 provide equalized reproduced signals and a Viterbi detector capable of receiving the

9 equalized reproduced signals and converting the reproduced signals into a digital output

10 signal indicative of data stored on a recording medium; wherein the equalizer is

11 implemented using a coefficient learning circuit that adaptively updates coefficients for

12 the equalizer based upon a cosine function, the equalizer adjusting coefficients using a

13 tap coefficient update equation having a first parameter, k, for modifying a magnitude

14 response, wherein the first parameter, k, is adjusted according to $k = k - g * (f(a_{k+1}) + f(a_{k-1})) * e_k$, where k is the cosine equalizer parameter for modifying the magnitude response, g

15 is an update attenuation gain, f() is a predetermined cosine function, a_{k+1} represents a bit

16 to be detected at time k+1, a_{k-1} represents a bit to be detected at time k-1, and e_k is an

17 error signal based on a difference between a noisy equalized signal and a desired

18 noiseless signal.

1 35-36. (Canceled)

1 37. (Currently Amended) The magnetic storage device of claim [[35]] 34,
2 wherein the equalizer adjusts coefficients using a tap coefficient update equation having a
3 second parameter, j, for modifying a phase response.

1 38. (Previously Presented) The magnetic storage device of claim 37,
2 wherein the second parameter, j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where
3 j is the cosine equalizer parameter for modifying the phase response, g is an update
4 attenuation gain, f() is a predetermined cosine function, a_{k+2} represents a bit to be
5 detected at time k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error
6 signal based on a difference between a noisy equalized signal and a desired noiseless
7 signal.

1 39. (Canceled)

1 40. (Currently Amended) ~~The magnetic storage device of claim 34 A~~
2 magnetic storage device, comprising:
3 a magnetic storage medium for recording data thereon;
4 a motor for moving the magnetic storage medium;
5 a head for reading and writing data on the magnetic storage medium;
6 an actuator for positioning the head relative to the magnetic storage medium; and
7 a data channel for processing encoded signals on the magnetic storage medium,
8 the data channel comprising an equalizer configured to equalize a digital signal to
9 provide equalized reproduced signals and a Viterbi detector capable of receiving the
10 equalized reproduced signals and converting the reproduced signals into a digital output
11 signal indicative of data stored on a recording medium; wherein the equalizer is
12 implemented using a coefficient learning circuit that adaptively updates coefficients for
13 the equalizer based upon a cosine function, wherein the coefficient learning circuit
14 adjusts coefficients, w_i , according to $w_i = w_i - g * f(a_{k-i}) * e_k$, where g is a provided update
15 attenuation gain and and $\{ f(a_{k-i}) \}$ $f(\cdot)$ is a predetermined cosine function and $\{ a_{k+i} \}$ a_k .
16 i represents a bit to be detected at time $\{ k+I \}$ $k-i$.

1 41. (Original) The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i} , are convolved
3 with a PR4 response based upon the cosine function.

1 42. (Original) The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i} + a_{k-i-1} \cdot a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are
3 convolved with the EPR4 response based upon the cosine function.

1 43. (Original) The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i}t_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with t_k
3 based upon the cosine function.

1 44. (Original) The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is
2 chosen to be $a_{k-i}h_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with h_k
3 based upon the cosine function.

1 45-46. (Canceled)